

# 74AHC123A-Q100; 74AHCT123A-Q100

Dual retriggerable monostable multivibrator with reset

Rev. 1 — 23 May 2013

Product data sheet

## 1. General description

The 74AHC123A-Q100; 74AHCT123A-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC123A-Q100; 74AHCT123A-Q100 are dual retriggerable monostable multivibrators with output pulse width control by three methods. The selection of an external resistor ( $R_{ext}$ ) and capacitor ( $C_{ext}$ ) program the basic pulse time. The external resistor and capacitor are normally connected as shown in [Figure 11](#).

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ( $n\bar{A}$ ) or the active HIGH-going edge input ( $nB$ ). By repeating this process, the output pulse period ( $nQ = \text{HIGH}$ ,  $n\bar{Q} = \text{LOW}$ ) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input  $n\bar{RD}$ , which also inhibits the triggering.

An internal connection from  $n\bar{RD}$  to the input gate makes it possible to trigger the circuit by a positive-going signal at input  $n\bar{RD}$  as shown in [Table 3](#), [Figure 8](#) and [Figure 9](#) illustrate pulse control by retriggering and early reset. The values of the external timing components  $R_{ext}$  and  $C_{ext}$ , determine the basic output pulse width. When  $C_{ext} \geq 10 \text{ nF}$ , the typical output pulse width is defined as:  $t_W = R_{ext} \times C_{ext}$  where  $t_W = \text{pulse width in ns}$ ;  $R_{ext} = \text{external resistor in k}\Omega$ ;  $C_{ext} = \text{external capacitor in pF}$ . Schmitt-trigger action at all inputs makes the circuit highly tolerant to slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$  and from  $-40 \text{ }^\circ\text{C}$  to  $+125 \text{ }^\circ\text{C}$
- All inputs have a Schmitt-trigger action
- Inputs accept voltages higher than  $V_{CC}$
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- For 74AHC123A-Q100 only: operates with CMOS input levels
- For 74AHCT123A-Q100 only: operates with TTL input levels
- ESD protection:



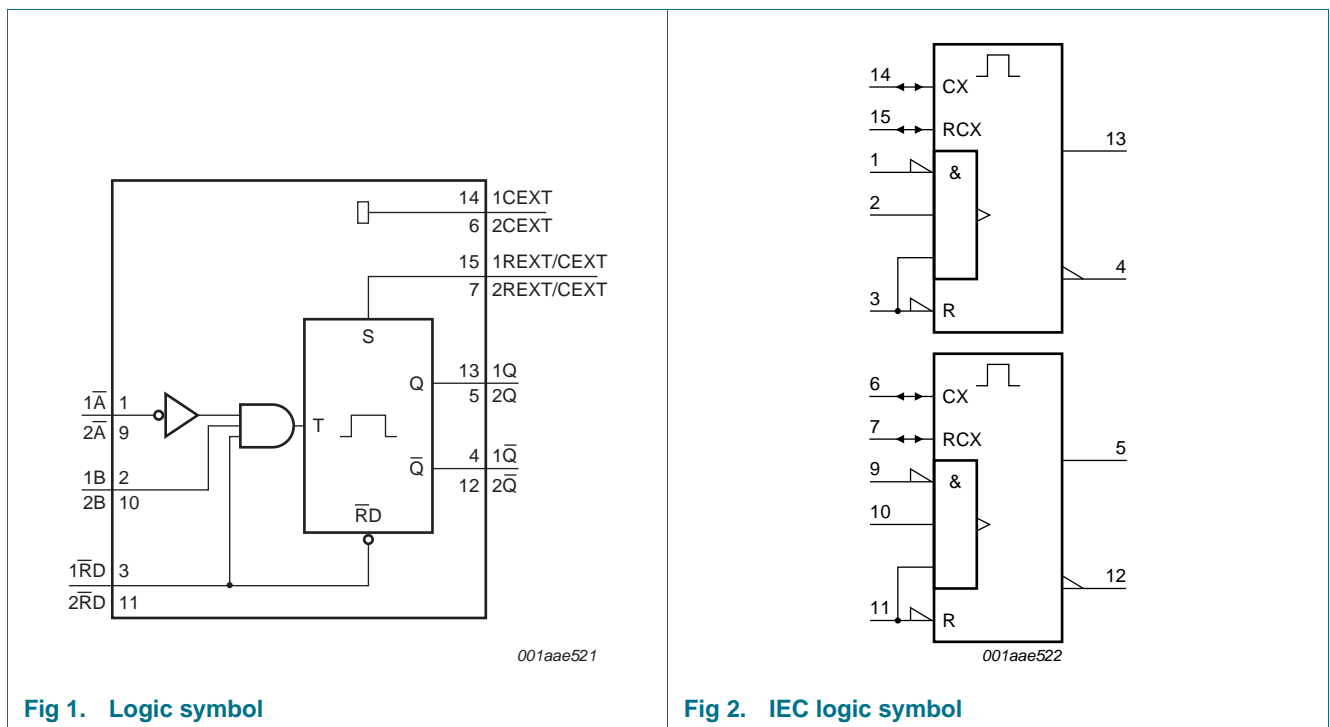
- ◆ MIL-STD-883, method 3015 exceeds 2000 V
- ◆ HBM JESD22-A114F exceeds 2000 V
- ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC123AD-Q100 74AHCT123AD-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC123APW-Q100 74AHCT123APW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC123ABQ-Q100 74AHCT123ABQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 4. Functional diagram



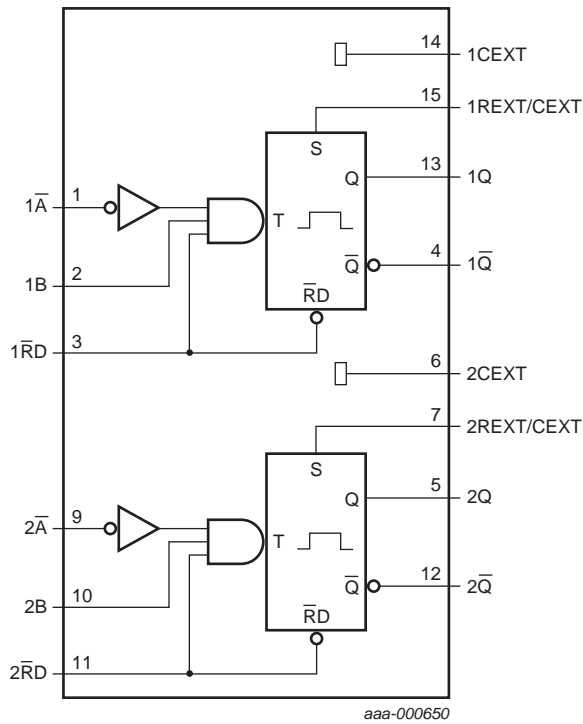
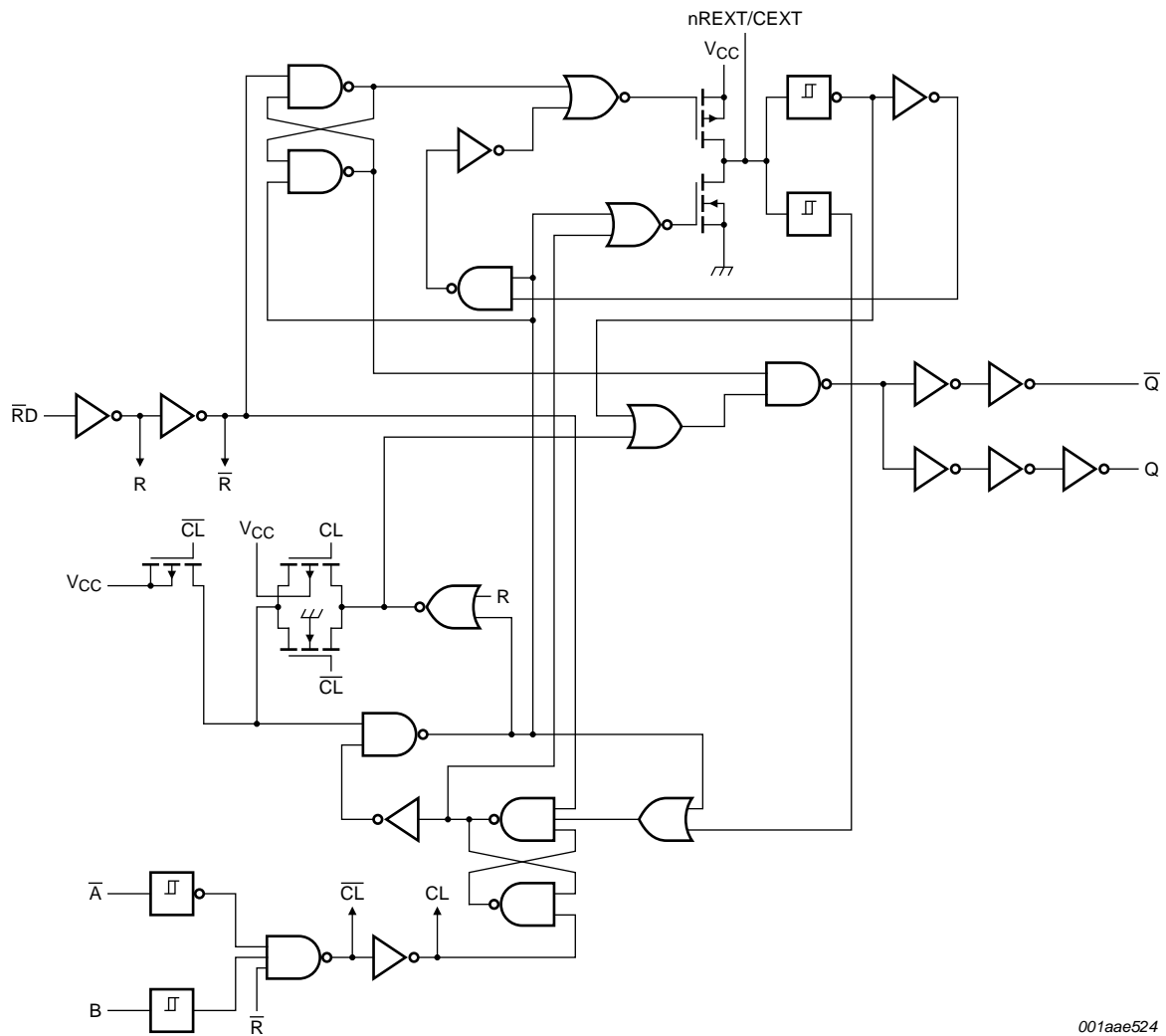


Fig 3. Functional diagram



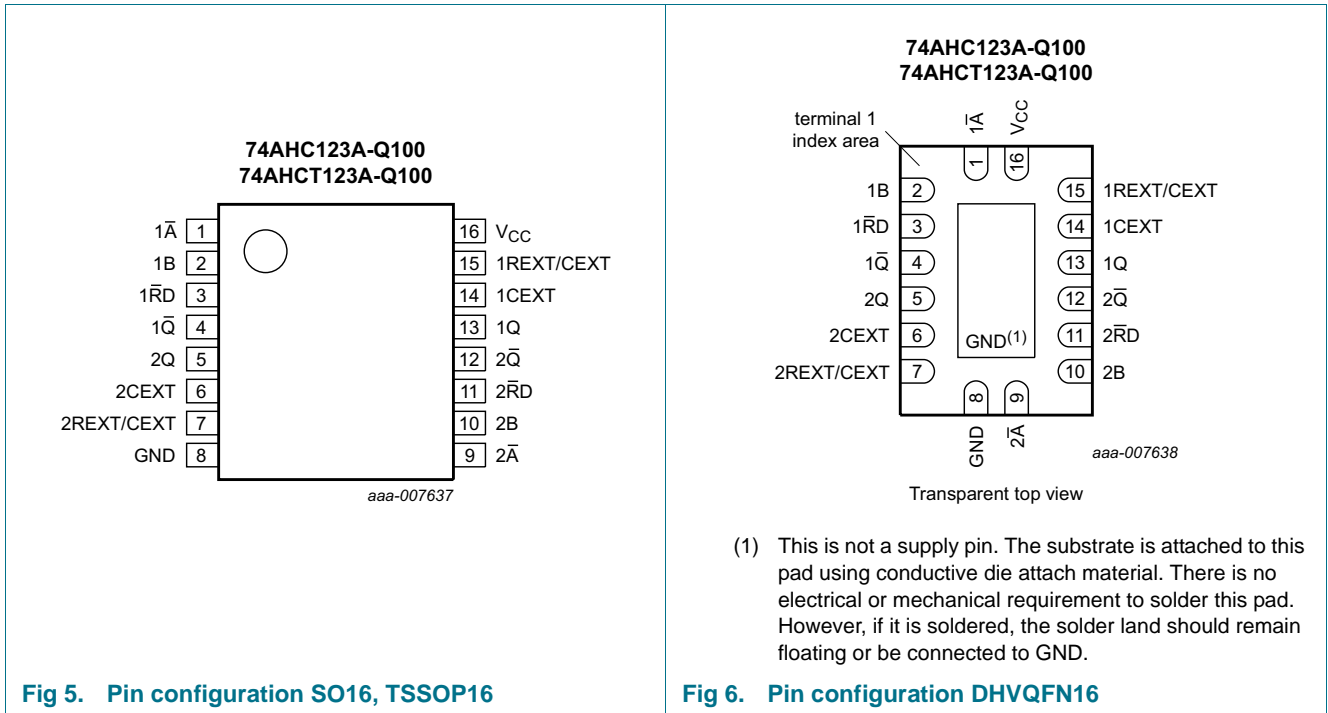
001aae524

For minimum noise generation, ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

Fig 4. Functional diagram

5. Pinning information

5.1 Pinning









5.2 Pin description

Table 2. Pin description


Symbol	Pin	Description
1 $\bar{A}$	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
1 $\bar{RD}$	3	direct reset LOW and positive-edge triggered input 1
1 $\bar{Q}$	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
2 $\bar{A}$	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
2 $\bar{RD}$	11	direct reset LOW and positive-edge triggered input 2
2 $\bar{Q}$	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V <sub>CC</sub>	16	supply voltage


## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input			Output	
nRD	nA	nB	nQ	nQ
L	X	X	L	H
X	H	X	L <sup>[2]</sup>	H <sup>[2]</sup>
X	X	L	L <sup>[2]</sup>	H <sup>[2]</sup>
H	L	↑		
H	↓	H		
↑	L	H		

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 ↑ = LOW-to-HIGH transition;  
 ↓ = HIGH-to-LOW transition;

 = one HIGH level output pulse;

 = one LOW level output pulse.

- [2] If the monostable multivibrator was triggered before this condition was established, the pulse continues as programmed.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	<sup>[1]</sup> -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	<sup>[1]</sup> -	±20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
	SO16 package		<sup>[2]</sup> -	500	mW
	TSSOP16 package		<sup>[3]</sup> -	500	mW
	DHVQFN16 package		<sup>[4]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.  
 [3] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.  
 [4] P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC123A-Q100			74AHCT123A-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
<b>74AHC123A-Q100</b>											
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V	
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V	
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V	
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V	
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V	
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>									
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V	
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V	
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V	
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V	
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>									
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V	
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V	
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V	
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V	
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V									
		nREXT/CEXT	<a href="#">11</a>	-	-	±0.25	-	±2.5	-	±10.0	μA
		pins nA, nB, nRD	-	-	±0.1	-	±1.0	-	±2.0	μA	

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA	
		active state (per circuit); V <sub>I</sub> = V <sub>CC</sub> or GND	[1]								
		V <sub>CC</sub> = 3.0 V	-	160	250	-	280	-	280	μA	
		V <sub>CC</sub> = 4.5 V	-	380	500	-	650	-	650	μA	
		V <sub>CC</sub> = 5.5 V	-	560	750	-	975	-	975	μA	
C <sub>I</sub>	input capacitance		-	5.0	10	-	10	-	10	pF	
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF	
<b>74AHCT123A-Q100</b>											
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V	
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V									
		I <sub>O</sub> = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V	
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V									
		I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V	
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V	
I <sub>I</sub>	input leakage current	nREXT/CEXT; V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	[1]								
		pins nA, nB, nRD; V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1.0	-	±2.0	μA	
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA	
		active state (per circuit); V <sub>I</sub> = V <sub>CC</sub> or GND	[1]								
		V <sub>CC</sub> = 4.5 V	-	380	500	-	650	-	650	μA	
		V <sub>CC</sub> = 5.5 V	-	560	750	-	975	-	975	μA	
C <sub>I</sub>	input capacitance		-	3	10	-	10	-	10	pF	
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF	

[1] Voltage on nREXT/CEXT = 0.5 × V<sub>CC</sub> and pin nREXT/CEXT in OFF-state during test.



## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V; For test circuit see Figure 12.*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit		
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max			
<b>74AHC123A-Q100</b>												
$t_{pd}$	propagation delay	$\overline{nA}$ and $nB$ to $nQ$ and $n\overline{Q}$ ; see Figure 7 <a href="#">[2]</a>	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$									
			$C_L = 15\text{ pF}$	-	7.4	20.6	1.0	24.0	1.0	26.0	ns	
			$C_L = 50\text{ pF}$	-	10.5	24.1	1.0	27.5	1.0	30.0	ns	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$										
		$C_L = 15\text{ pF}$	-	5.1	12.0	1.0	14.0	1.0	15.5	ns		
		$C_L = 50\text{ pF}$	-	7.3	14.0	1.0	16.0	1.0	17.5	ns		
		$\overline{nRD}$ to $nQ$ and $n\overline{Q}$ ; see Figure 7 <a href="#">[2]</a>	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$									
			$C_L = 15\text{ pF}$	-	8.2	22.4	1.0	26.0	1.0	28.0	ns	
			$C_L = 50\text{ pF}$	-	11.7	25.9	1.0	29.5	1.0	32.0	ns	
			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$									
			$C_L = 15\text{ pF}$	-	5.6	12.9	1.0	15.0	1.0	16.5	ns	
			$C_L = 50\text{ pF}$	-	8.1	14.9	1.0	17.0	1.0	19.0	ns	
		$\overline{nRD}$ to $nQ$ and $n\overline{Q}$ (reset); see Figure 7 <a href="#">[2]</a>	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$									
			$C_L = 15\text{ pF}$	-	6.4	15.8	1.0	18.5	1.0	20.0	ns	
			$C_L = 50\text{ pF}$	-	9.2	19.3	1.0	22.0	1.0	24.5	ns	
$V_{CC} = 4.5\text{ V to }5.5\text{ V}$												
$C_L = 15\text{ pF}$	-		4.4	9.4	1.0	11.0	1.0	12.0	ns			
$C_L = 50\text{ pF}$	-		6.3	11.4	1.0	13.0	1.0	14.5	ns			

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V; For test circuit see Figure 12.*

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
t <sub>w</sub>	pulse width	inputs; n $\bar{A}$ = LOW; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; nB = HIGH; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; n $\bar{RD}$ = LOW; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		outputs; n $\bar{Q}$ = LOW and nQ = HIGH; C <sub>L</sub> = 50 pF; see <a href="#">Figure 7</a> , <a href="#">Figure 8</a> , <a href="#">Figure 9</a> and <a href="#">Figure 10</a>		<a href="#">[3]</a>						
		C <sub>ext</sub> = 28 pF; R <sub>ext</sub> = 2 k $\Omega$								
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	115	240	-	300	-	300	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	100	200	-	240	-	240	ns
		C <sub>ext</sub> = 0.01 $\mu$ F; R <sub>ext</sub> = 10 k $\Omega$								
		V <sub>CC</sub> = 3.0 V to 3.6 V	90	100	110	90	110	85	115	$\mu$ s
		V <sub>CC</sub> = 4.5 V to 5.5 V	90	100	110	90	110	85	115	$\mu$ s
C <sub>ext</sub> = 0.1 $\mu$ F; R <sub>ext</sub> = 10 k $\Omega$ ;										
V <sub>CC</sub> = 3.0 V to 3.6 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms		
V <sub>CC</sub> = 4.5 V to 5.5 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms		
t <sub>trig</sub>	retrigger time	n $\bar{A}$ to nB; C <sub>ext</sub> = 100 pF; R <sub>ext</sub> = 1 k $\Omega$ ; C <sub>L</sub> = 50 pF; see <a href="#">Figure 8</a> and <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	60	-	-	-	-	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	39	-	-	-	-	ns	
		n $\bar{A}$ to nB; C <sub>ext</sub> = 0.01 $\mu$ F; R <sub>ext</sub> = 1 k $\Omega$ ; C <sub>L</sub> = 50 pF; see <a href="#">Figure 8</a> and <a href="#">Figure 10</a>								
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	1.5	-	-	-	-	$\mu$ s	
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	-	-	-	-	$\mu$ s	
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>i</sub> = GND to V <sub>CC</sub>	<a href="#">[4]</a>	-	57	-	-	-	pF	

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V; For test circuit see [Figure 12](#).*

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max		
<b>74AHCT123A-Q100</b>											
$t_{pd}$	propagation delay	$n\bar{A}$ and $nB$ to $nQ$ and $n\bar{Q}$ ; see <a href="#">Figure 7</a> <sup>[2]</sup>									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$									
		$C_L = 15\text{ pF}$	-	5.0	12.0	1.0	14.0	1.0	15.5	ns	
		$C_L = 50\text{ pF}$	-	7.1	14.0	1.0	16.0	1.0	17.5	ns	
		$n\bar{RD}$ to $nQ$ and $n\bar{Q}$ ; see <a href="#">Figure 7</a> <sup>[2]</sup>									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$									
	propagation delay	propagation delay	$n\bar{RD}$ to $nQ$ and $n\bar{Q}$ ; see <a href="#">Figure 7</a> <sup>[2]</sup>								
			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
			$C_L = 15\text{ pF}$	-	5.2	12.9	1.0	15.0	1.0	16.5	ns
			$C_L = 50\text{ pF}$	-	7.5	14.9	1.0	17.0	1.0	18.5	ns
			$n\bar{RD}$ to $nQ$ and $n\bar{Q}$ (reset); see <a href="#">Figure 7</a> <sup>[2]</sup>								
			$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
$t_w$	pulse width	inputs; $n\bar{A} = \text{LOW}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 7</a>									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns	
		inputs; $nB = \text{HIGH}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 7</a>									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns	
		inputs; $n\bar{RD} = \text{LOW}$ ; $C_L = 50\text{ pF}$ ; see <a href="#">Figure 7</a>									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns	
		outputs; $n\bar{Q} = \text{LOW}$ and $nQ = \text{HIGH}$ ; $C_L = 50\text{ pF}$ ; $C_{ext} = 28\text{ pF}$ ; $R_{ext} = 2\text{ k}\Omega$ ; see <a href="#">Figure 7</a> , <a href="#">Figure 8</a> , <a href="#">Figure 9</a> and <a href="#">Figure 10</a> <sup>[3]</sup>									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	100	200	-	240	-	240	ns	
		$C_{ext} = 0.01\text{ }\mu\text{F}$ ; $R_{ext} = 10\text{ k}\Omega$									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	90	100	110	90	110	85	115	$\mu\text{s}$	
		$C_{ext} = 0.1\text{ }\mu\text{F}$ ; $R_{ext} = 10\text{ k}\Omega$									
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0.9	1	1.1	0.9	1.1	0.85	1.15	ms	

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V; For test circuit see Figure 12.*

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
t <sub>trig</sub>	retrigger time	nA to nB; C <sub>ext</sub> = 100 pF; R <sub>ext</sub> = 1 kΩ; C <sub>L</sub> = 50 pF; see Figure 8 and Figure 10								
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	60	-	-	-	-	-	ns
C <sub>PD</sub>	power dissipation capacitance	nA to nB; C <sub>ext</sub> = 0.01 μF; R <sub>ext</sub> = 1 kΩ; C <sub>L</sub> = 50 pF; see Figure 8 and Figure 10								
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.5	-	-	-	-	-	μs
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>i</sub> = GND to V <sub>CC</sub>	[4]	58	-	-	-	-	-	pF

**External components**

R <sub>ext</sub>	external resistance	V <sub>CC</sub> = 2.0 V	5	-	-	-	-	-	-	kΩ
		V <sub>CC</sub> > 3.0 V	1	-	-	-	-	-	-	kΩ
C <sub>ext</sub>	external capacitance	V <sub>CC</sub> = 2.0 V	[5]	-	-	-	-	-	-	pF
		V <sub>CC</sub> > 3.0 V	[5]	-	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; C<sub>ext</sub> = 0 pF; R<sub>ext</sub> = 5 kΩ.

[3] For C<sub>ext</sub> ≥ 10 nF, the typical value of the pulse width t<sub>W</sub> (μs) = C<sub>ext</sub> (nF) × R<sub>ext</sub> (kΩ).

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

[5] C<sub>ext</sub> has no limits.

11. Waveforms

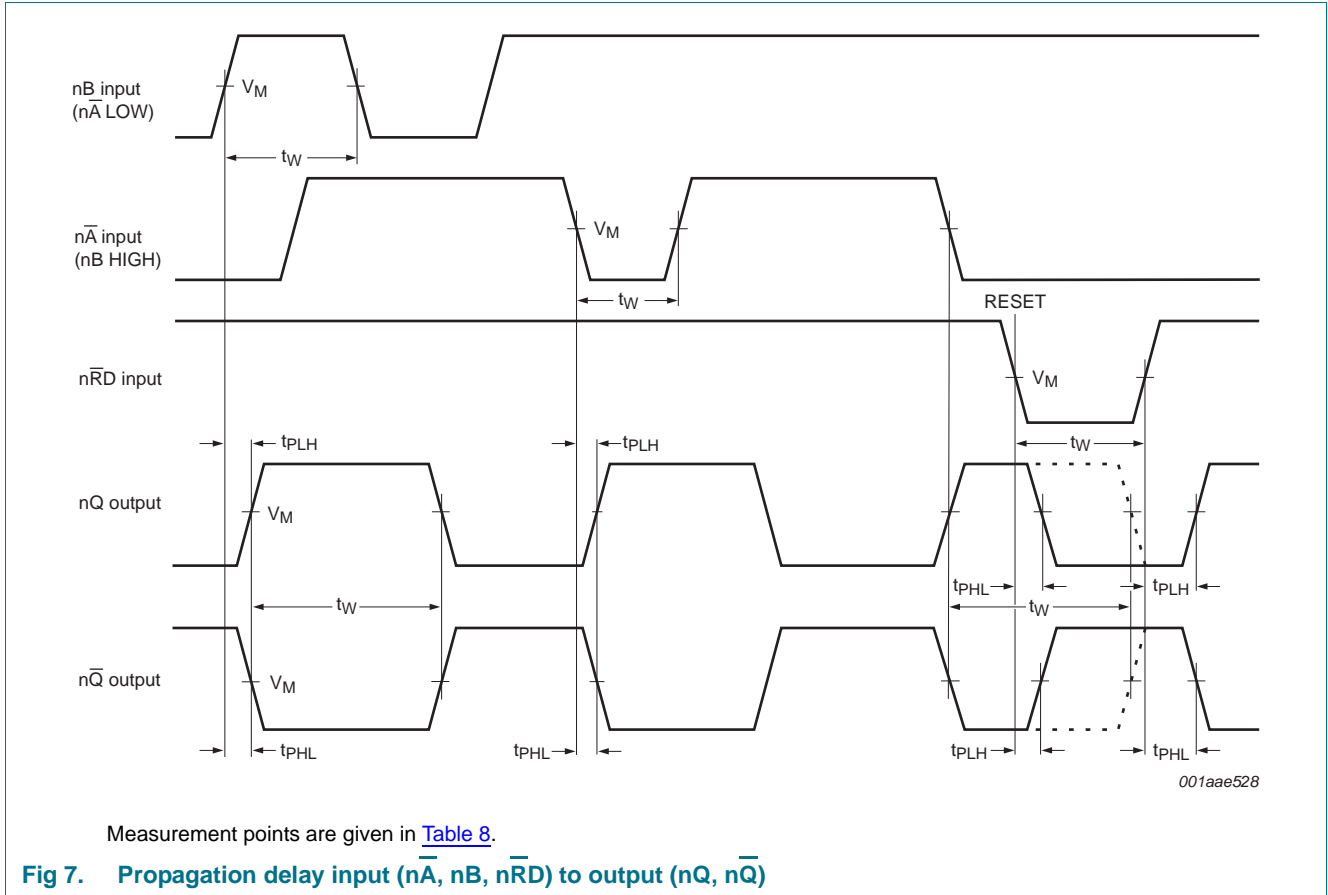
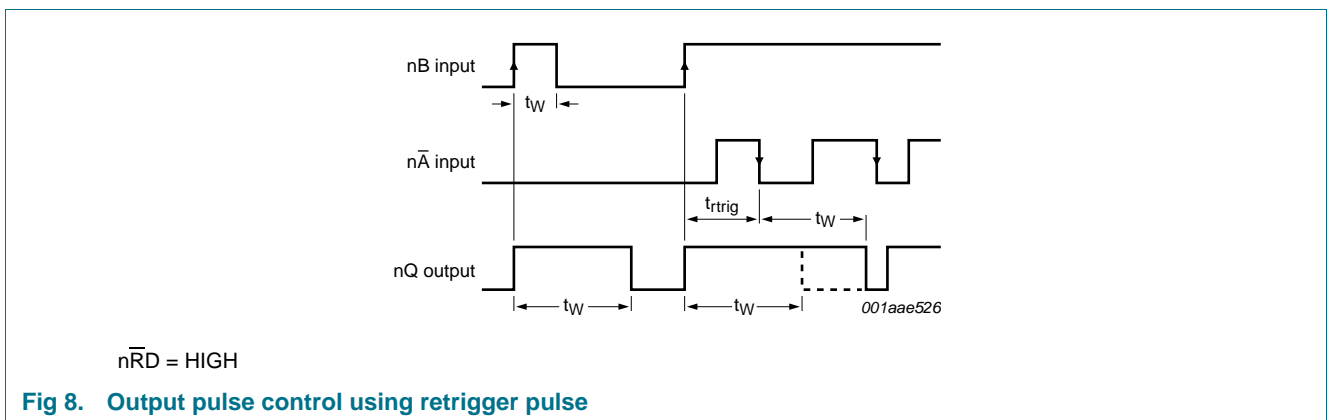
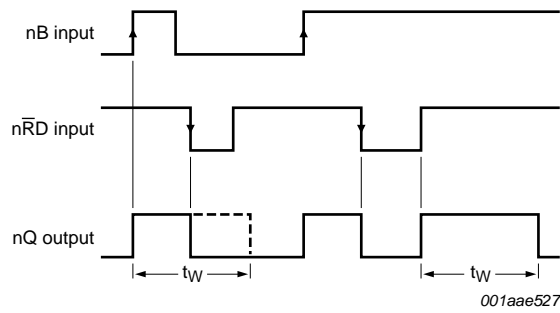


Table 8. Measurement points

Type	Input	Output
	$V_M$	$V_M$
74AHC123A-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT123A-Q100	1.5 V	$0.5V_{CC}$





$\bar{nA} = \text{LOW}$

Fig 9. Output pulse control using reset input  $\bar{nRD}$

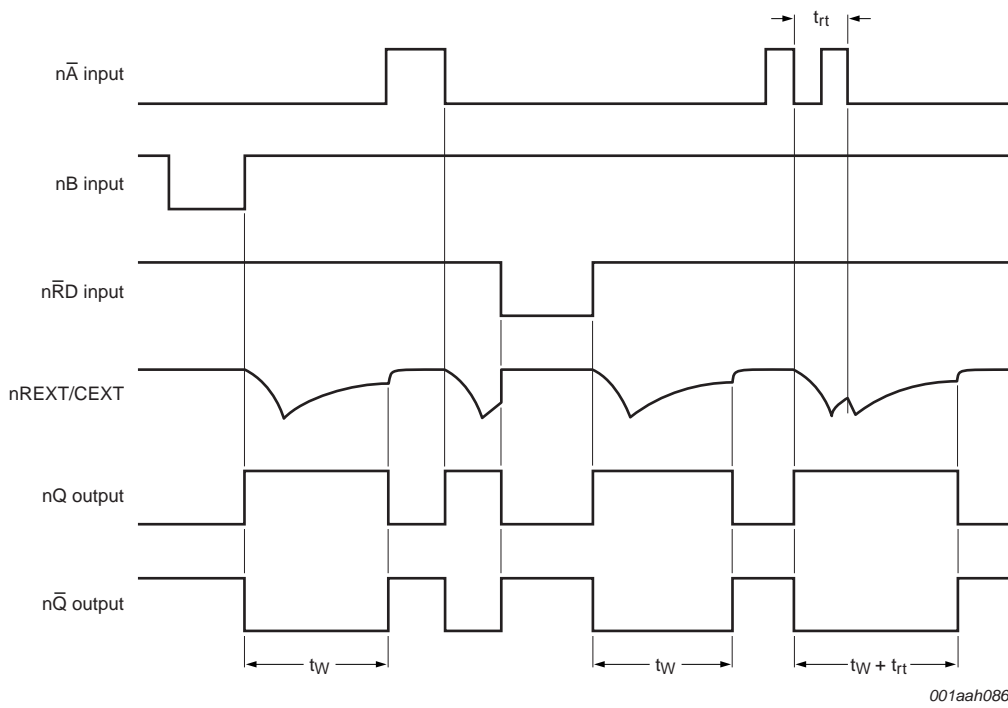


Fig 10. Input and output timing

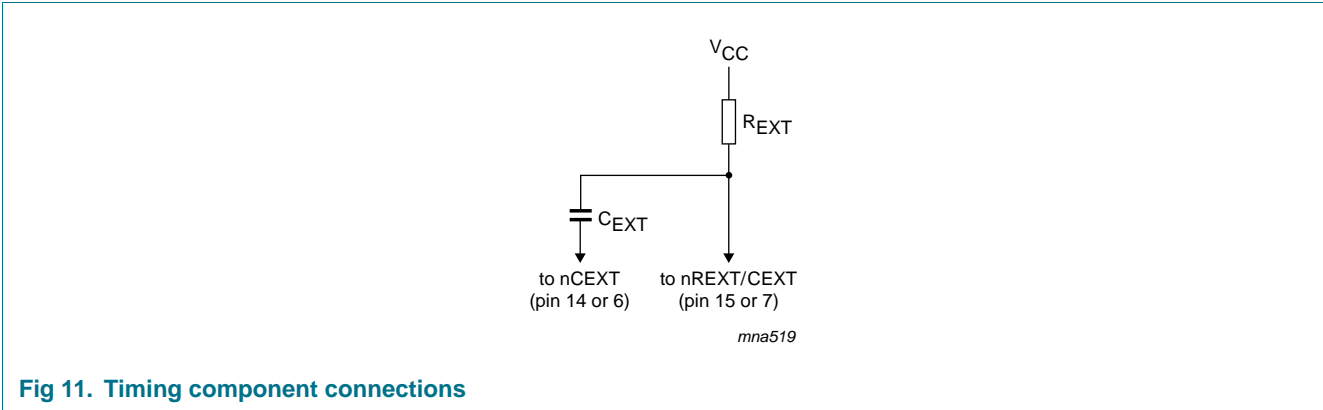
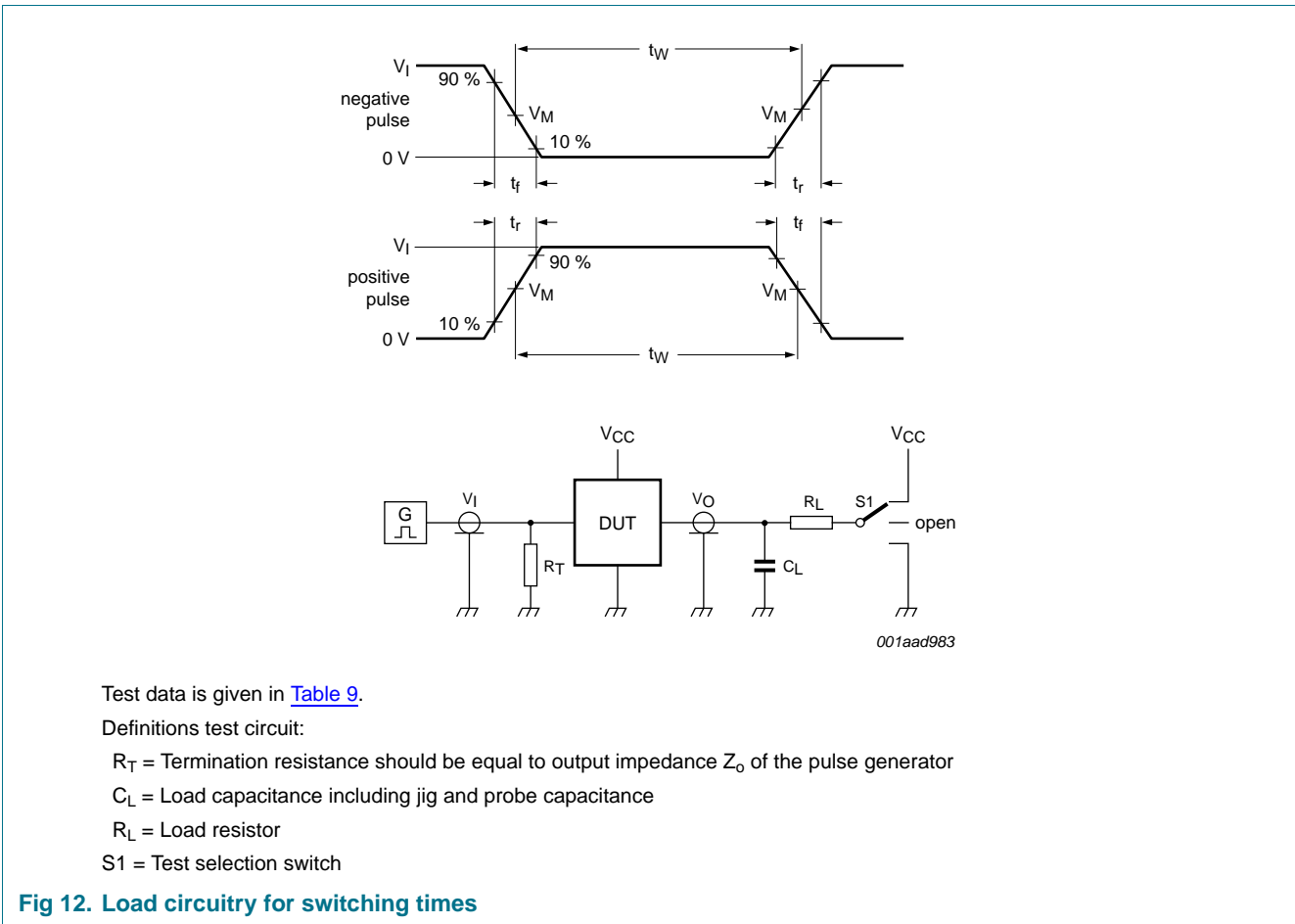


Fig 11. Timing component connections



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator

$C_L$  = Load capacitance including jig and probe capacitance

$R_L$  = Load resistor

$S_1$  = Test selection switch

Fig 12. Load circuitry for switching times

Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC123A-Q100	$V_{CC}$	3.0 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT123A-Q100	3.0 V	3.0 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

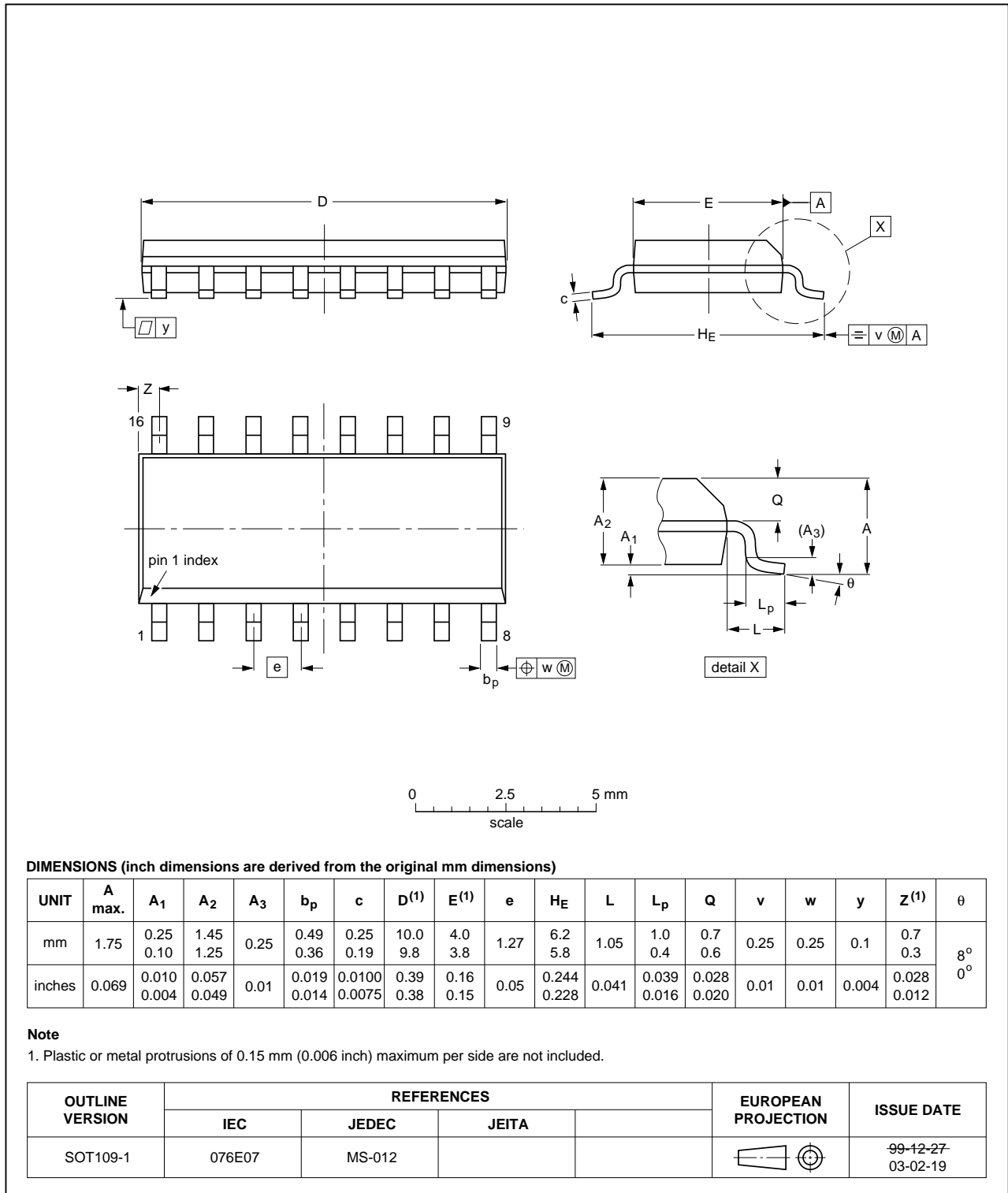


Fig 13. Package outline SOT109-1 (SO16)



TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

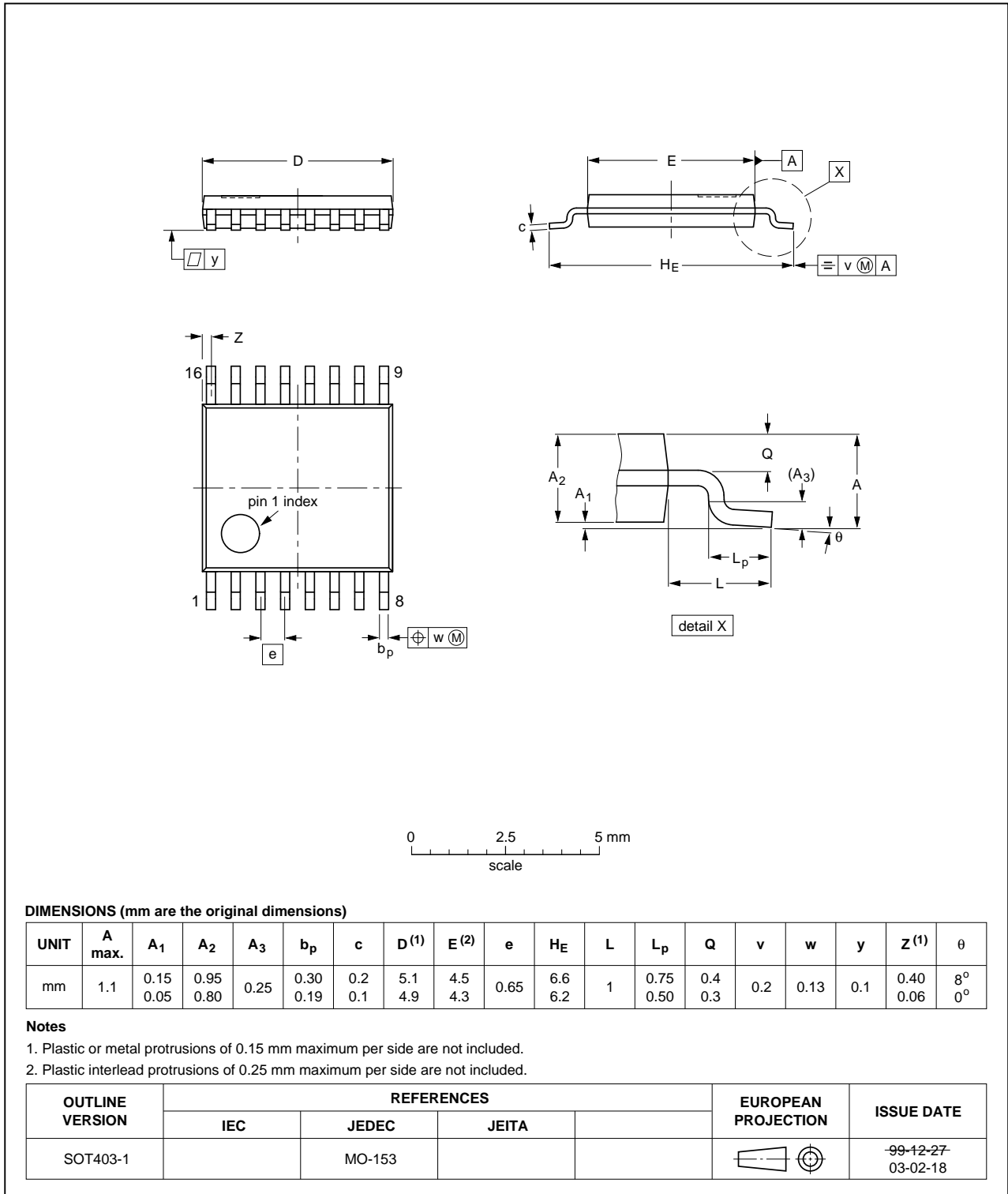


Fig 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

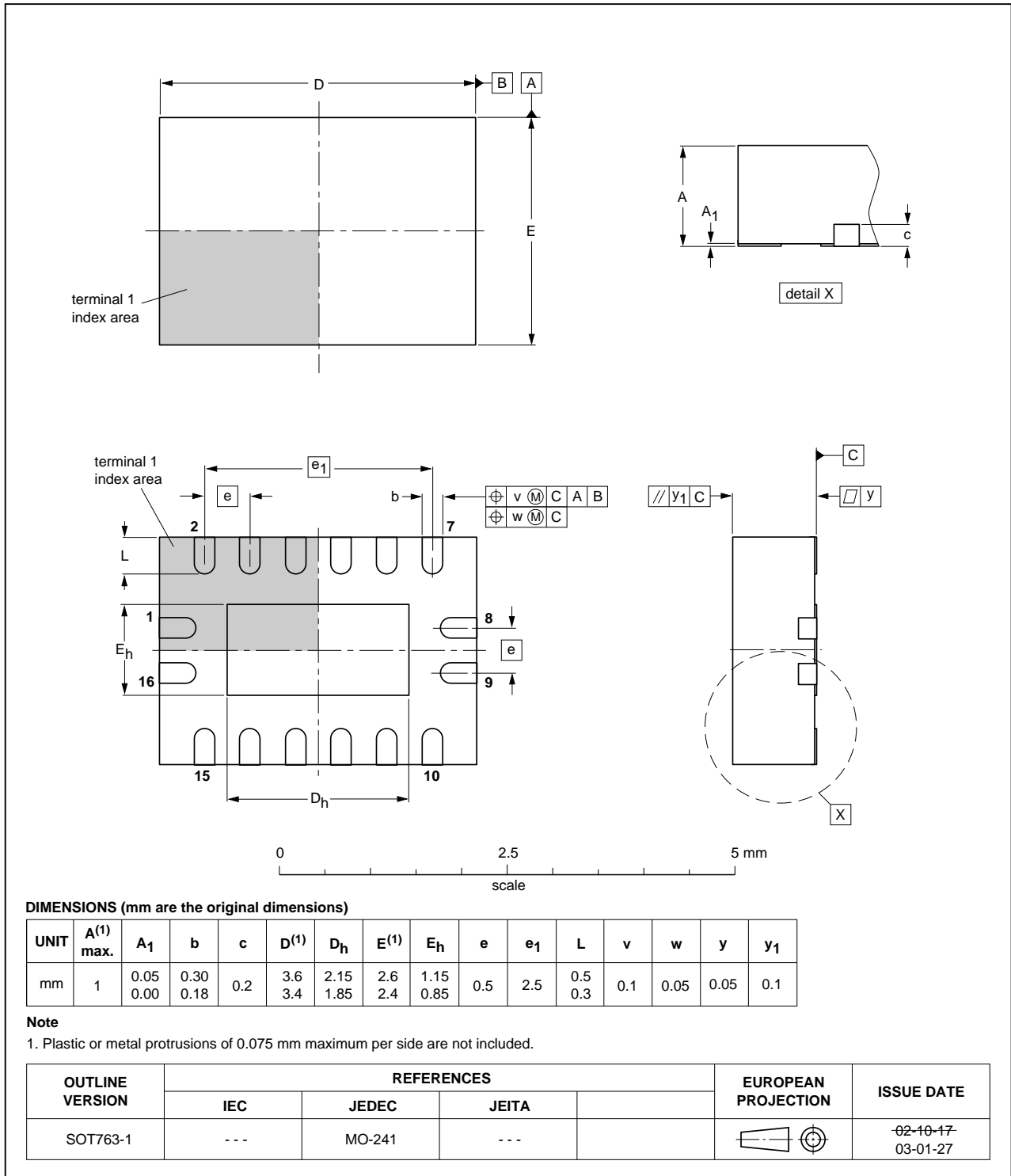


Fig 15. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT123A_Q100 v.1	20130523	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 15.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 17. Contents

---

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>5</b>
5.1	Pinning .....	5
5.2	Pin description .....	5
<b>6</b>	<b>Functional description</b> .....	<b>6</b>
<b>7</b>	<b>Limiting values</b> .....	<b>6</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>7</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>7</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>9</b>
<b>11</b>	<b>Waveforms</b> .....	<b>13</b>
<b>12</b>	<b>Package outline</b> .....	<b>16</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>19</b>
<b>14</b>	<b>Revision history</b> .....	<b>19</b>
<b>15</b>	<b>Legal information</b> .....	<b>20</b>
15.1	Data sheet status .....	20
15.2	Definitions .....	20
15.3	Disclaimers .....	20
15.4	Trademarks .....	21
<b>16</b>	<b>Contact information</b> .....	<b>21</b>
<b>17</b>	<b>Contents</b> .....	<b>22</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 23 May 2013

Document identifier: 74AHC\_AHCT123A\_Q100